PRODUCT SPECIFICATION

H256NN-S

Wi-Fi Dual-band 1x1 802.11 a/b/g/n

Module Datasheet

Version:V1.0

Customer: _____

Customer P/N:_____

Signature:_____

Date:_____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

TEL: +86-755-2955-8186 Website: www.fn-link.com

H256NN-S Module Datasheet

	Part NO.	Description
Ordering Information	FGH256NNSX-K1	SV6256P,802.11a/b/g/n,1T1R ,13*13.5 ,SDIO2.0,ipex 座子
	FGH256NNSX-01	SV6256P,802.11a/b/g/n,1T1R ,13*13.5 ,SDIO2.0,ipex 座子

CONTENTS

Revision History

Version	Date	Contents of Revision Change	Draft	Checked	Approved
V1.0	2023/07/21	New version	TZQ	LXY	Qjp

1. General Description

1.1 Introduction

H256NN-S is a low-power module with the highest level of integration for internet of thing embedded systems. It is designed to support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11n MCS0~MCS7, HT20/HT40, 800ns and 400ns guard interval.

The Main chip WLAN is designed to support IEEE 802.11 a/b/g/n single stream with the state of-the-art design techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile and handheld devices. The Main chip WLAN low power function uses the innovative design techniques and the optimized architecture which best utilizes the advanced process technology to reduce active and idle power, and achieve extreme low power consumption at sleep state to extend the battery life. The Main chip WLAN A-MPDU Tx function maximizes the throughput performance while achieving the best buffer utilization.

1.2 Description

Model Name	H256NN-S
Product Description	Support Wi-Fi functionalities
Dimension	L x W x H: 13 x 13.5 x2.0 mm
Wi-Fi Interface	Support SDIO V2.0
Operating temperature	-10°C to 70°C
Storage temperature	-40°C to 85°C

2. Features

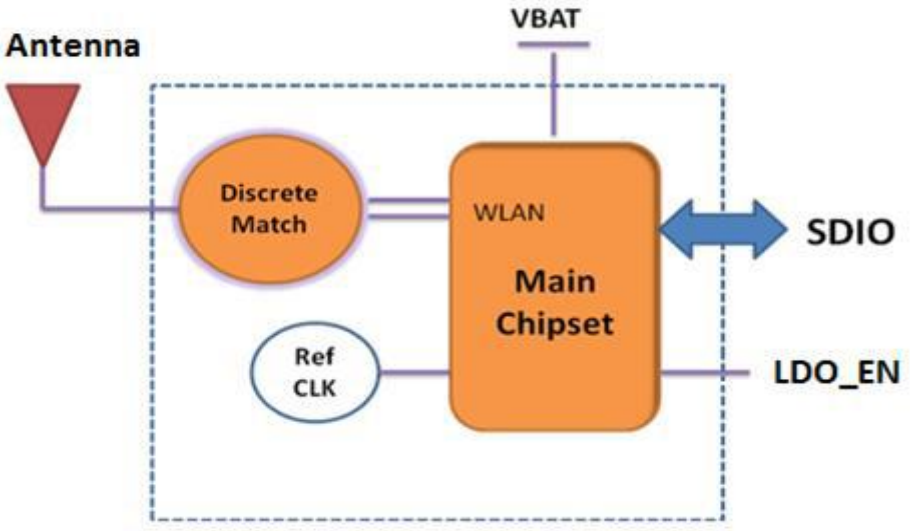
General Features

- support IEEE 802.11 a/b/g/n single stream
- Single stream 802.11n provides highest throughput and superior RF performance for embedded system .
- ntegrated dual-band WLAN CMOS efficient power amplifier with internal power detector and closed loop power calibration
- Enhanced and robust sensitivity for wider coverage range

Host Interface

- Supports popular interfaces: SDIO 2.0 (50MHz, 4-bit and 1-bit) / SPI

3. Block Diagram



4. General Specification

4.1 2.4GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 20dBm ± 2 dB	EVM ≤ -10dB
	802.11g /54Mbps : 14dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 14dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
Test Items	**TYP Test Value**	**Standard Value**
Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps PER @ -95 dBm	≤-83
	- 2Mbps PER @ -93 dBm	≤-80
	- 5.5Mbps PER @ -91 dBm	≤-79
	- 11Mbps PER @ -88 dBm	≤-76
Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps PER @ -91 dBm	≤-85
	- 9Mbps PER @ -90 dBm	≤-84
	- 12Mbps PER @ -88 dBm	≤-82
	- 18Mbps PER @ -86 dBm	≤-80
	- 24Mbps PER @ -82 dBm	≤-77
	- 36Mbps PER @ -79 dBm	≤-73
	- 48Mbps PER @ -74 dBm	≤-69
	- 54Mbps PER @ -73 dBm	≤-68
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -91 dBm	≤-85
	- MCS=1 PER @ -88 dBm	≤-82
	- MCS=2 PER @ -86 dBm	≤-80
	- MCS=3 PER @ -81 dBm	≤-77
	- MCS=4 PER @ -79 dBm	≤-73
	- MCS=5 PER @ -74 dBm	≤-69
	- MCS=6 PER @ -73 dBm	≤-68
	- MCS=7 PER @ -68 dBm	≤-67
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0, PER @ -88 dBm	≤-82
	- MCS=1, PER @ -85 dBm	≤-79

	- MCS=2, PER @ -83 dBm	≤-77
	- MCS=3, PER @ -78 dBm	≤-74
	- MCS=4, PER @ -76 dBm	≤-70
	- MCS=5, PER @ -71 dBm	≤-66
	- MCS=6, PER @ -70 dBm	≤-65
	- MCS=7, PER @ -67 dBm	≤-64
Maximum Input Level	802.11b : -10 dBm	
	802.11g/n : -20 dBm	

4.2 5GHz RF Specification

Feature	**Description**	
WLAN Standard	IEEE 802.11 a/n Wi-Fi compliant	
Frequency Range	5.15 GHz ~ 5.85 GHz (5.0 GHz Band)	
Number of Channels	5.0GHz：Please see the table1	
Test Items	**Typical Value**	**EVM**
Output Power[1]	802.11a /54Mbps : 11dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7(HT20) : 11dBm ± 2 dB	EVM ≤ -28dB
	802.11n /MCS7(HT40) : 11dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
Test Items	**Test Value**	**Standard Value**
SISO Receive Sensitivity (11a,20MHz) @10% PER	- 6Mbps PER @ -87 dBm	≤-85 dBm
	- 9Mbps PER @ -86 dBm	≤-84 dBm
	- 12Mbps PER @ -85 dBm	≤-82 dBm
	- 18Mbps PER @ -84 dBm	≤-80 dBm
	- 24Mbps PER @ -82 dBm	≤-77 dBm
	- 36Mbps PER @ -78 dBm	≤-73 dBm
	- 48Mbps PER @ -75 dBm	≤-69 dBm
	- 54Mbps PER @ -73 dBm	≤-68 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -87 dBm	≤-85 dBm
	- MCS=1 PER @ -84 dBm	≤-82 dBm
	- MCS=2 PER @ -82 dBm	≤-80 dBm
	- MCS=3 PER @ -80 dBm	≤-77 dBm
	- MCS=4 PER @ -77 dBm	≤-73 dBm
	- MCS=5 PER @ -74 dBm	≤-69 dBm

	- MCS=6	PER @ -72 dBm	≤-68 dBm
	- MCS=7	PER @ -70 dBm	≤-67 dBm
SISO Receive Sensitivity (11n ,40MHz) @10% PER	- MCS=0	PER @ -87 dBm	≤-82 dBm
	- MCS=1	PER @ -84 dBm	≤-79 dBm
	- MCS=2	PER @ -81 dBm	≤-77 dBm
	- MCS=3	PER @ -78 dBm	≤-74 dBm
	- MCS=4	PER @ -75 dBm	≤-70 dBm
	- MCS=5	PER @ -72 dBm	≤-66 dBm
	- MCS=6	PER @ -70 dBm	≤-65 dBm
	- MCS=7	PER @ -68 dBm	≤-64 dBm
Maximum Input Level	802.11a: -10 dBm		
	802.11n: -20 dBm		

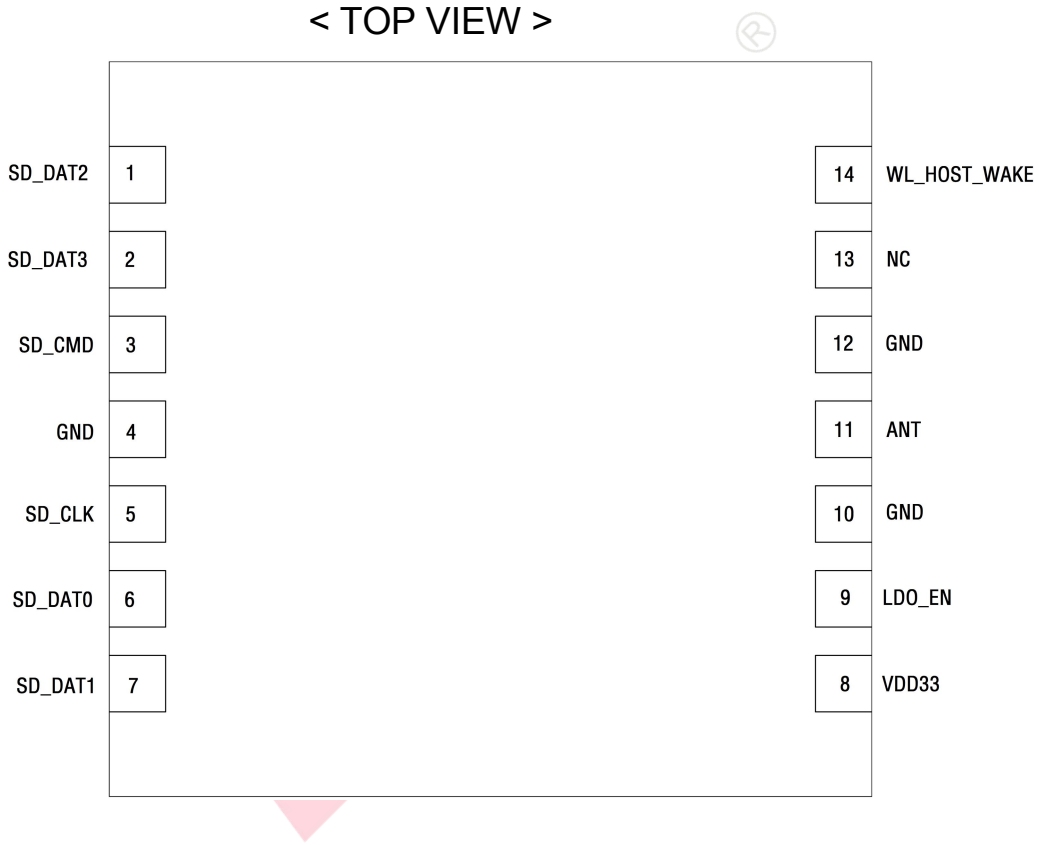
[1]5GHz(20MHz) Channel table

Band range	Operating Channel Numbers	Channel center frequencies(MHz)
5150MHz~5250MHz	36	5180
	40	5200
	44	5220
	48	5240
5250MHz~5350MHz	52	5260
	56	5280
	60	5300
	64	5320
5470MHz~5725MHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640
	132	5660
	136	5680
	140	5700
5725MHz~5850MHz	149	5745
	153	5765

	157	5785
	161	5805
	165	5825

5. Pin Definition

5.1 Pin Outline



5.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	SD_DAT2	I/O	SDIO data line 2	
2	SD_DAT3	I/O	SDIO data line 3	
3	SD_CMD	I/O	SDIO command line	
4	GND		Ground connections	
5	SD_CLK	I	SDIO clock line	
6	SD_DAT0	I/O	SDIO data line 0	
7	SD_DAT1	I/O	SDIO data line 1	

8	VDD33		3.3V	
9	LDO_EN		Enable pin for WLAN device Defualt ON: pull high ; OFF: pull low	
10	GND		Ground connections	
11	ANT	I/O	RF I/O port (NC)	
12	GND		Ground connections	
13	NC		Floating (NC)	
14	WL_HOST_WAKE	O	WLAN wake up HOST	

P:POWER I:INPUT O:OUTPUT

6. Electrical Specifications

6.1 Power Supply DC Characteristics

	MIN	TYP	MAX	Unit
Operating Temperature	-10	25	70	deg.C
VDD33	3.0	3.3	3.6	V

6.2 Power Consumption

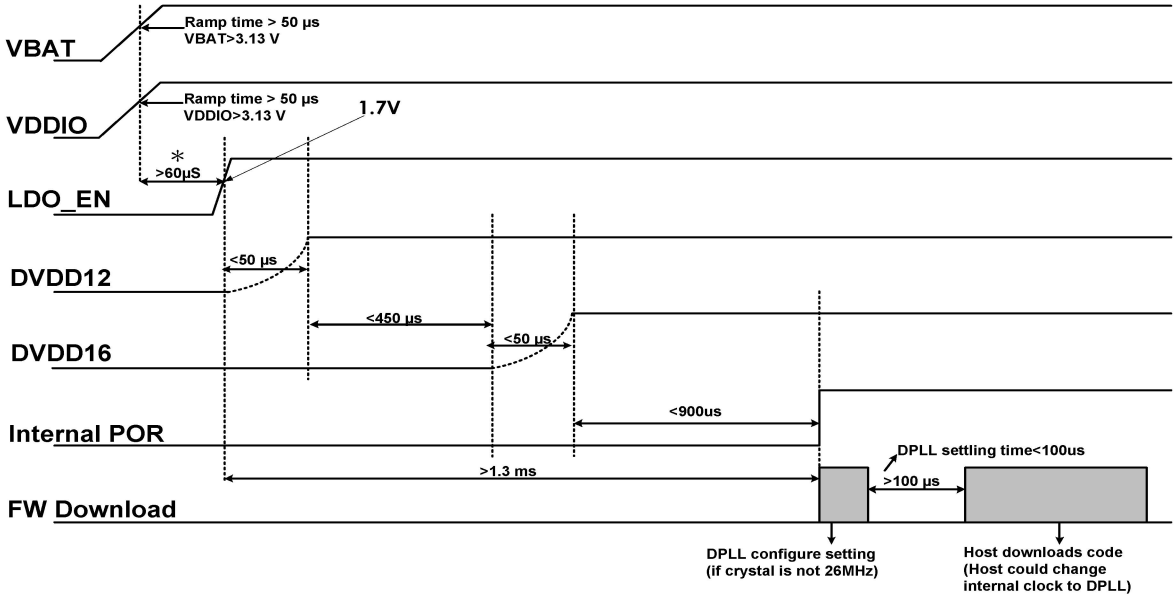
Power Consumption (Typical by using SWR)	Wi-Fi only: TBD

6.3 Power-on sequence

shows the power-on sequence of the SV6256P from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept the same as VDDIO voltage level. After initial power-on, the LDO_EN signal can be held low to turn off the SV6256P or pulsed low to induce a subsequent reset. After LDO_EN is assert and host starts the power-on sequence of the SV6256P. From that point, the typical SV6256P power-on sequence is shown below:

1. Within 1.3 millisecond, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.

2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.



Note: For IOT application, the timing between VDDIO and LDO_EN should be greater than [external flash VCC (min) to /CS Low+ 60us]. For example, if we use W25Q16JV as external flash, the timing between VDDIO and LDO_EN should be greater than (20us+60us).

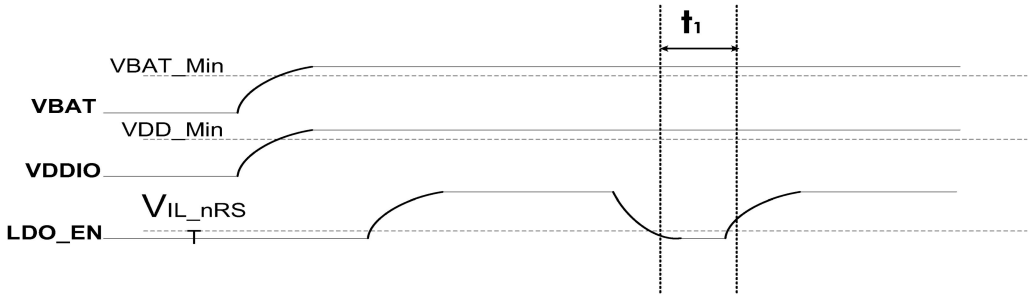


Figure 5 : Reset Timing

Table 2: Reset Timing Parameters

Parameters	Description	Min.	Unit
t_1	Duration of LDO_EN signal level < V_{IL}_nRST to reset the chip	30	us

6.4 Interface Circuit time series

6.4.1 SDIO TIMING WAVEFORM

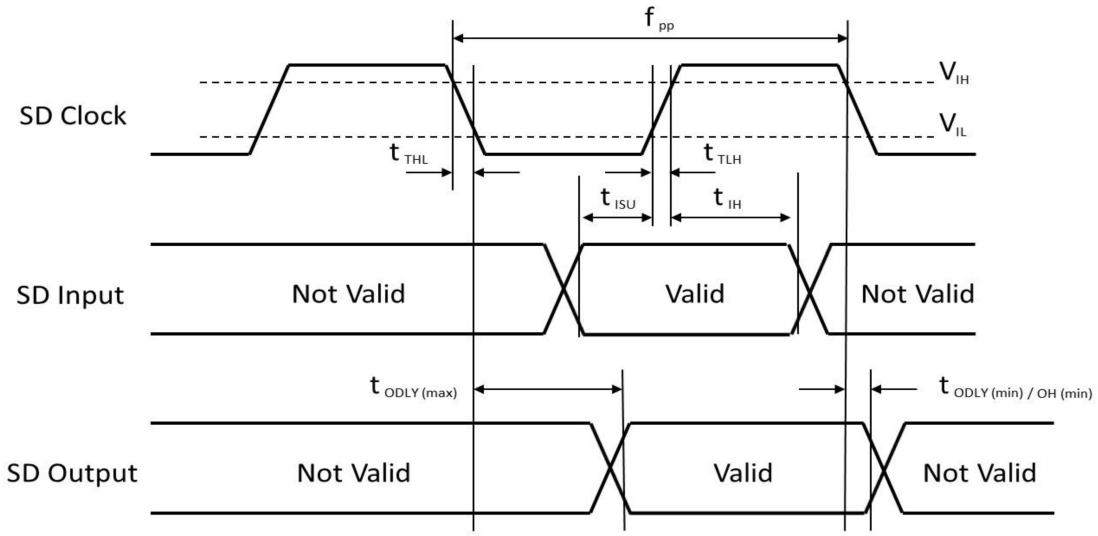


Table 4: SDIO version 2.0 Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Clock CLK (All values are referred to min(V_{IH}) and max (V_{IL}).					
f_{pp}	Clock frequency Data Transfer Mode	0		50	MHz
t_{TLH}	Clock rise time			3	ns
t_{THL}	Clock fall time			3	ns
Inputs CMD, DAT (reference to CLK)					
t_{ISU}	Input set-up time	6			ns
t_{IH}	Input hold time	2			ns
Outputs CMD, DAT (reference to CLK)					
t_{ODLY}	Output Delay time during Data Transfer Mode			14	ns
t_{OH}	Output Hold time	2.5			Ns

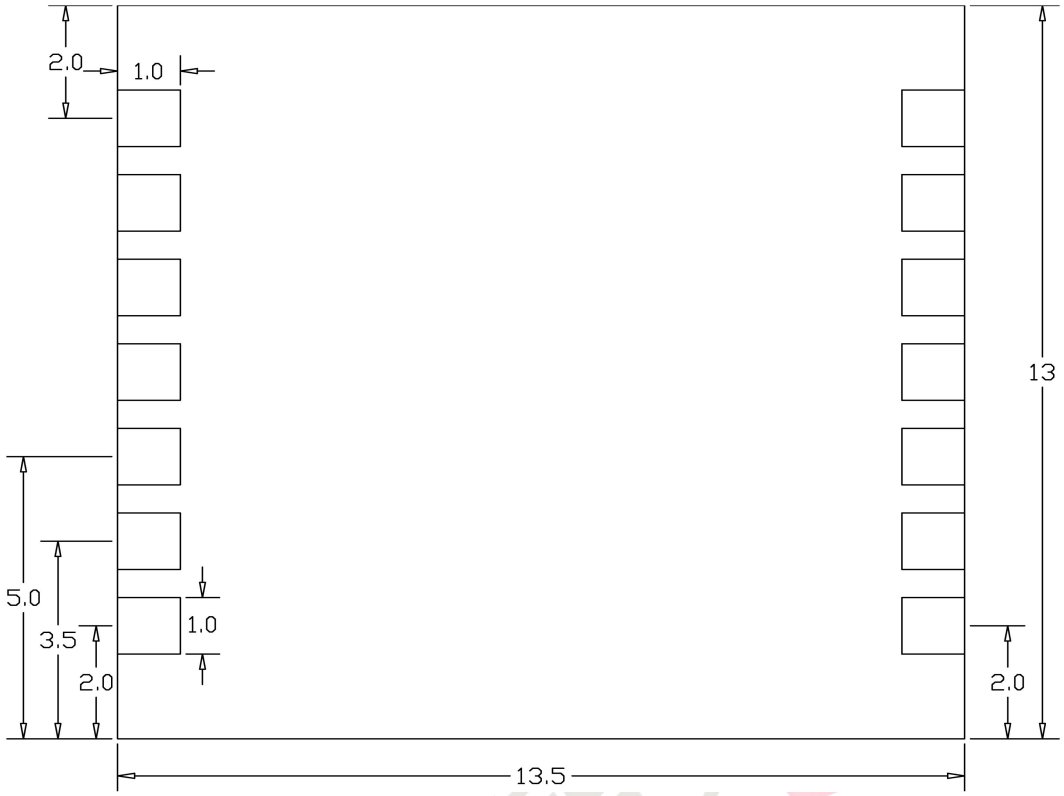
7. Size reference

7.1 Module Picture

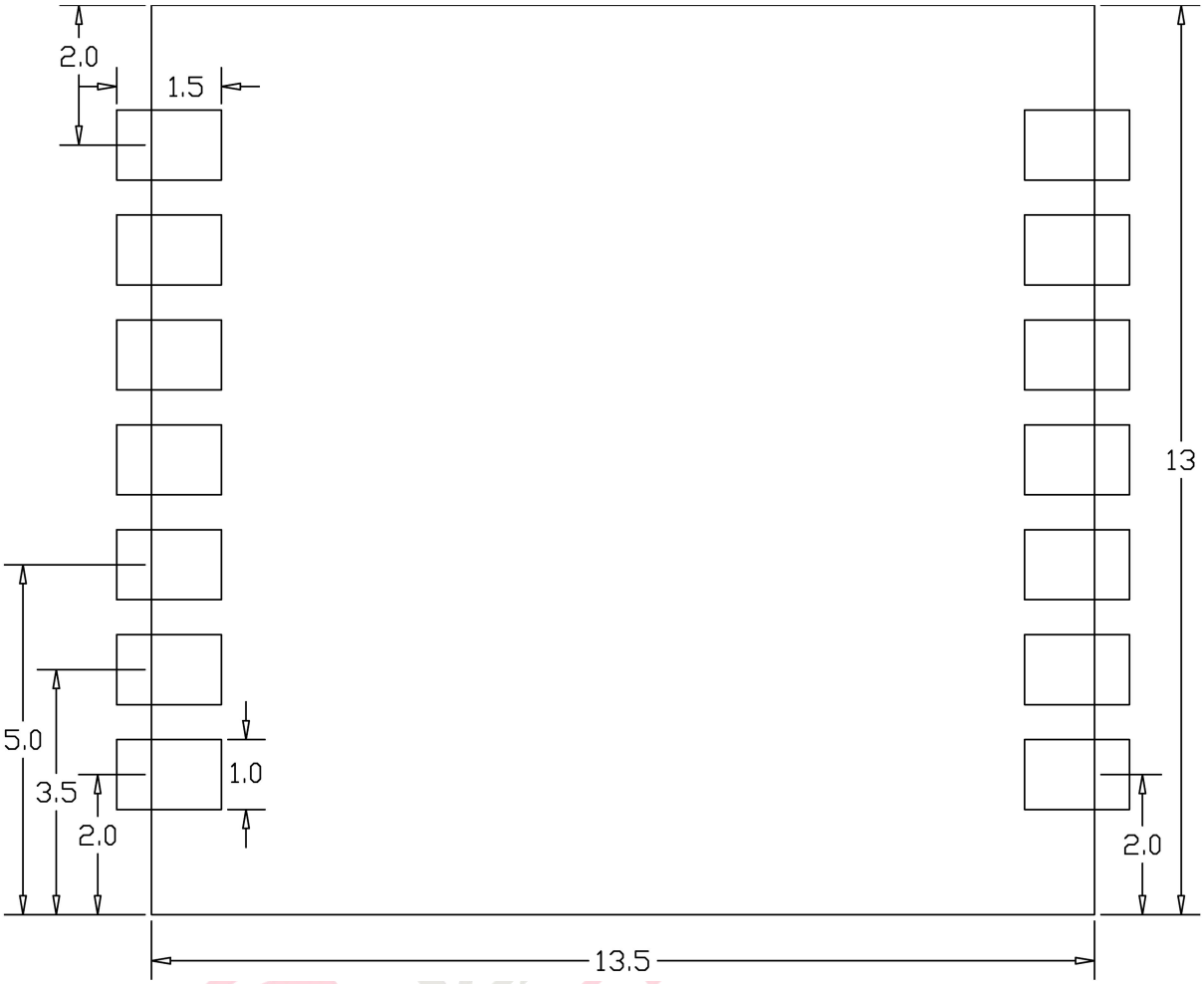
<table>
<tr><td>L x W : 13 x 13.5 (+0.3/-0.1) mm
FGH256NNSX-K1
  
FGH256NNSX-01
   </td><td>  </td></tr>
<tr><td>H: 2.0 (±0.2) mm</td><td>  </td></tr>
<tr><td>Weight</td><td>0.50g</td></tr>
</table>

7.2 Physical Dimensions

<TOP View>


2.0
1.0
13
5.0
3.5
2.0
1.0
2.0
13.5

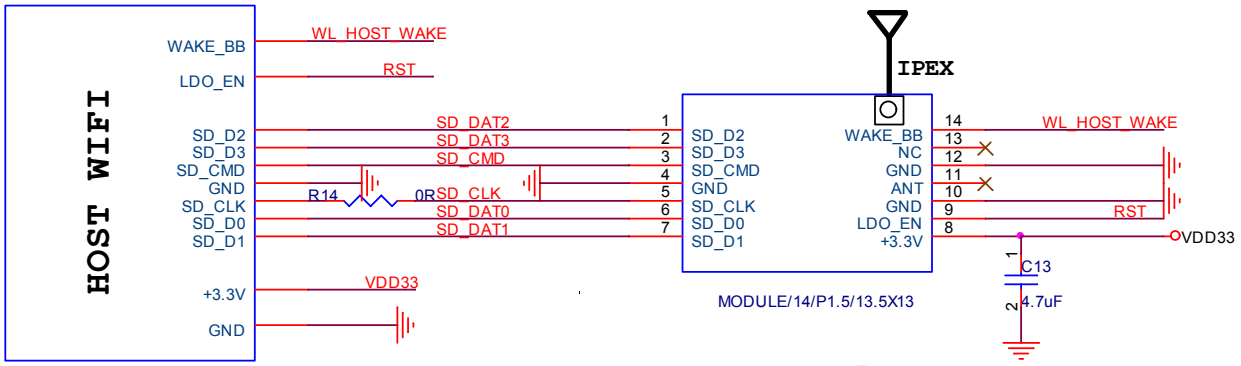
7.3 Layout Recommendation



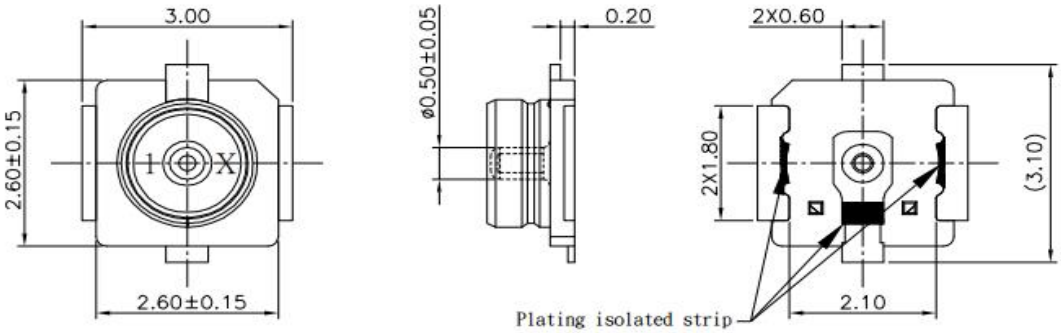
8. The Key Material List

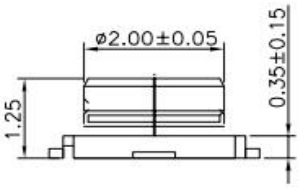
Item	Part Name	Description	Manufacturer
1	PCB	H256NN-S,4L,FR4,13X13.5X0.8mm	XY-PCB, GDKX, Sunlord, SLPCB，TRULY
2	Crystal	3225 24MHZ CL=8pF,10ppm	ECEC, Hosonic, TKD, JWT
3	Chipset	SV6256P, QFN48L	iComm-semi
4	IPEX	1 代 UFLR-MINIPCL	佳沃，创迪尔,启明盛

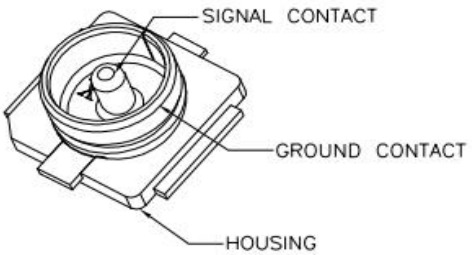
9. Reference Design



Ipex Information





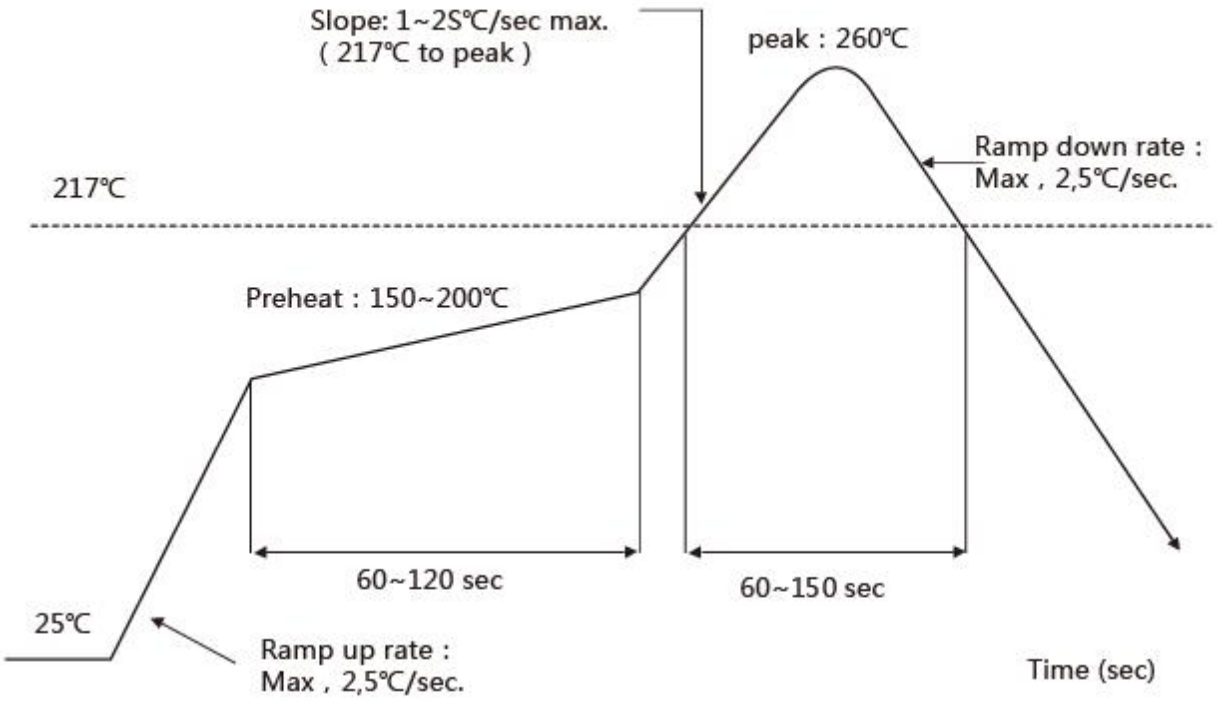


10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260°C

Number of Times : ≤2 times



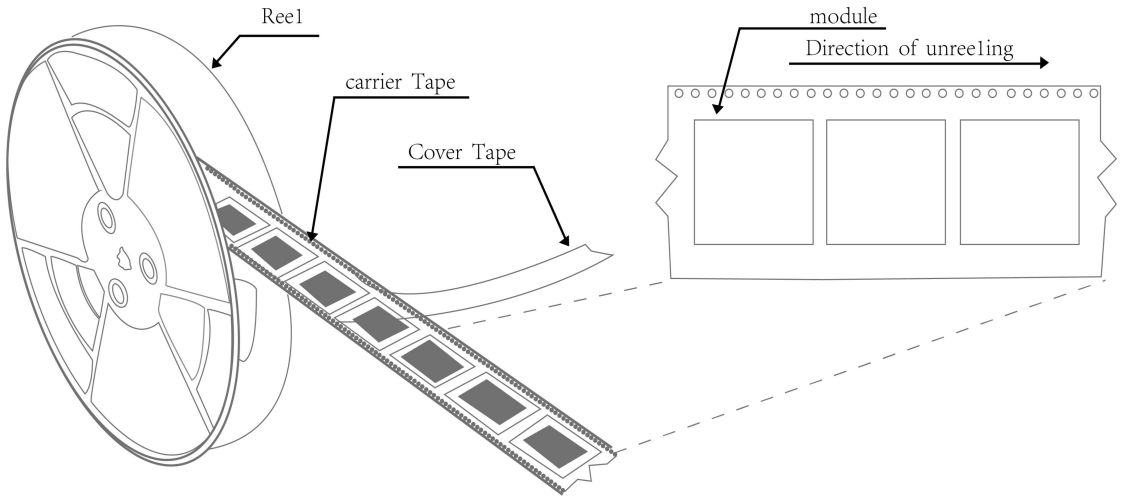
11. RoHS compliance

All hardware components are fully compliant with EU RoHS directive

12. Package

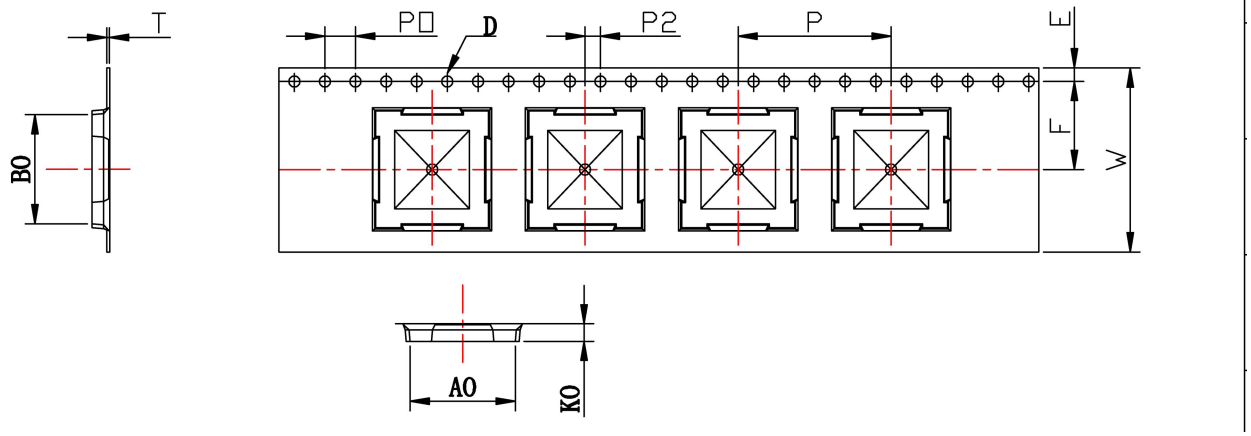
12.1 Reel

A roll of 1500pcs



12.2 Carrier Tape Detail

ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	13.35	13.95	1.50	11.5	1.75	2.30	4.0	2.0	20.0	0.30
TOLE	+0.3 -0.3	±0.15	±0.15	+0.1 -0.0	+0.1 -0.1	±0.1	±0.10	±0.1	±0.1	±0.1	±0.05



12.3 Packaging Detail

the take-up package

Using self-adhesive tape

Size of black tape: 24mm*24.4m the cover tape :21.3mm*32.6m

Color of plastic disc: blue

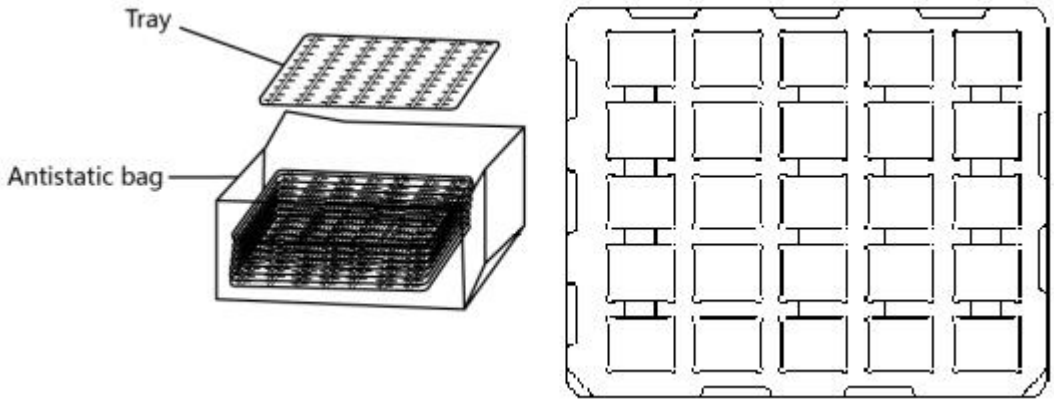
NY bag size:450mm*415mm

size ： 350*350*35mm

The packing case size:360*210*370mm

12.4 Tray

Use pallet packaging for less than 300 pieces



13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

d) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

e) Baking is required if conditions b) or c) are not respected

f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more